SYSTRON DONNER CORPORATION

MODEL 8230
TIME CODE READER

Instruction Manual

ELECTRONIC AND INERTIAL INSTRUMENTATION FOR MEASUREMENT, SIMULATION, CONTROL

MODEL 8230
TIME CODE READER

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TABLE OF CONTENTS

			page
CHAPTER 1	GENERAL DESCRIPTION		
	1.1	Introduction	1-1
	1.2	Features	1-2
	1.3	Specifications	1-3
	1.4	Options	1-5
CHAPTER 2	INSTALLATION		
	2.1	Initial Inspection	2-1
	2.2	Storage and Reshipment	2-1
	2.3	Power Requirements	2-2
	2.4	Installation	2-3
	2.5	Initial Turn On	2-3
	2.6	Tilt-Stand Removal	2-3
	2.7	Panel Installation/Cover Removal Procedure	2-4
CHAPTER 3	OPERATION		
	3.1	General	3-1
	3.2	Operating Conditions	3-1
CHAPTER 4	MAINTENANCE		
	4.1	Factory Service	4-1
	4.2	Routine Maintenance	4-1
	4.3	Printed-Circuit Board Repair	4-2
CHAPTER 5	FUNCTIONAL DESCRIPTION		
	5.1	General	5-1
	5.2	Code Stripper and Signal Conditioner	5-1
	5.3	Reader Logic	5-4
	5.4	Storage and Display	5-11
	5.5	Power Supply	5-12
CHAPTER 6	PARTS LIST AND ILLUSTRATIONS		
	6.1	Parts List	6-1
21981-4-1		Line Filter Assembly	6-4
31119-4-1		Time Code Reader Assembly	6-5
31119-7-1		Time Code Reader Schematic	6-6
31529-7-1	Sh. 1	Timing Diagram IRIG B	6-7
31529-7-1	Sh. 2	Timing Diagram IRIG B	6-8
		IRIG Time Code Formats	6-9

CHAPTER 1

GENERAL DESCRIPTION

1.1 Introduction

The Model 8230 Time Code Reader is essentially a time code translator designed to accept a serial BCD code in the forward direction on an amplitude modulated carrier. It converts this serial code into parallel form for display in hours, minutes and seconds. As an option, parallel BCD outputs can be made available at a rear connector.

The basic unit translates IRIG A, B or E code formats without the need for switching or code plug removal. Optional configurations are available for translating other IRIG, NASA or XR 3 code formats in lieu of the IRIG A, B and E codes.

The time display is updated two digits at a time as the time information is stripped from the serial input code. Storage is provided to eliminate flicker. If desired, "ON TIME" operation can be provided as an optional feature.

The small, lightweight, rugged housing combined with the swivel mounted pedestal (tilt stand) permits unique four-in-one mounting in racks or consoles, on benches or desktops, or tilt-mounted on top of equipment or on the wall.

The Model 8230 can be used in a wide variety of applications where data must be retrieved from magnetic tape recordings for purposes of access and identification during playback. One particularly valuable application is as a remote time display in situations where time information must be displayed at widely separated locations. A single coaxial line is used as opposed to 20 or more lines required for other types of displays.

1.2 Features

The Model 8230 is designed for simple, reliable operation and ease of maintenance. Most circuitry is contained on a single printed circuit board to minimize hand wiring. All silicon solid state components are used throughout. Integrated circuits are used wherever possible.

The unit is completely self-contained requiring only the serial input code and a source of 115/230 volts, 48-440 Hz power. It dissipates less than 12 watts and requires essentially no power from the signal source.

Long-life, in-line, neon-glow numerical indicators are used for front panel display. Lighted colons are provided between the hours, minutes and seconds elements in the readout to reduce the possibility of misinterpretation.

The only control is a front panel mounted ON-OFF switch.

The unit includes digital filtering and parallel data storage.

1.3 Specifications

Display

Six digit in-line readout to indicate time-of-day in hours, minutes and seconds. Numerals are 0.610" (15.5 mm) high.

Code Format

IRIG A, B or E codes are translated in the basic unit. Only time-of-day information in hours, minutes and seconds is stripped from the code. Any other information such as tenths of seconds, days, control functions, etc. is ignored. Other IRIG, NASA or XR 3 codes can be translated by optional configurations of the Model 8230.

Input

An amplitude modulated time code in the forward direction with a frequency from 50 Hz to 100 kHz and modulation ratios (mark to space) from 2:1 to 6:1 is accepted. Input levels must be between 0.75 volts and 20 volts peak-to-peak. Input impedance is greater than 1 MΩ via rear panel BNC connector.

Outputs (Optional)

Parallel BCD (8-4-2-1) in time-of-day. The seconds, minutes and hours are updated in order as the corresponding data is stripped

from the serial input code. Parallel outputs (and display) which are updated "on time" can be provided as an optional feature.

Logic Levels:	Binary "1" = 5 volts nominal Binary "0" = 0 volts nominal 15 mA sink
Connector:	Rear Panel Winchester

Manual Controls

Front Panel ON-OFF toggle switch (Power)

Environment

0° to +50°C at up to 95% relative humidity.

Power

115/230 volts (±10%) 48 to 440 Hz, 12 watts via rear panel connector. Cable supplied.

Dimensions

3-1/4" high x 7" wide x 8-1/8" deep (8.2 x 17.8 x 19.6 cm). Add 3-1/4 inches to height for tilt stand. For rack mounting, unit requires panel cutout of 3.110" high x 6.820" wide (7.9 x 17.3 cm).

Weight

Five pounds. (2.3 kg) shipping.

Accessories Furnished

Tilt stand and pedestal, 3 conductor power cord and instruction handbook furnished with each Model 8230. Optional rack mounting hardware is available.

1.4 Options

Option DII

Parallel BCD outputs. Time is provided as twenty parallel BCD lines representing hours, minutes and seconds at a rear panel connector.

Option EI8

Provides for the updating of the translated time code "on time". Usually combined with Option DII.

CHAPTER 2

INSTALLATION

2.1 Initial Inspection

As soon as the instrument is received, verify that it is intact and as ordered. Inspect the instrument for damage and if any shipping damage is found refer to the warranty inside the rear cover of this manual, and to subsection 2.2 for repackaging and shipping instructions.

As soon as possible, the instrument should be installed and given a thorough electrical inspection. Should the instrument fail to operate properly or fail to meet the listed specifications, immediately contact your Systron-Donner representative.

2.2 Storage and Reshipment

Environmental conditions during storage and shipment should be limited as follows:

Maximum Temperature: 185°F (85°C)

Minimum Temperature: -69°F (-55°C)

To protect your instrument during shipment or storage, use the best packaging methods available. Your Systron-Donner field office can provide materials similar to those used for original factory packaging. Contract packaging companies can provide dependable packaging on short notice.

General packaging instructions:

(1) Wrap the instrument in heavy paper or plastic before

placing it in the shipping container.

(2) If possible, use the original container designed for the instrument. Otherwise, use a strong carton (350 lb./sq. in. bursting strength) or a wooden box to house the instrument.

(3) Use plenty of packaging material around all sides of the instrument and protect the front panel with cardboard strips.

(4) Seal the package with strong tape or metal bands. Mark the package with "DELICATE INSTRUMENT".

(5) Refer to the warranty inside the rear cover of this manual and check with your Systron-Donner field office for shipping instructions. All correspondence should refer to the instrument by its model number and full serial number.

2.3 Power Requirements

The Model 8230 can operate from 115 V or 230 V ±10%, 48 to 440 Hz, 12 watts. The unit is normally shipped with jumper connections for 115 volt operation. To adapt it for 230 volt operation, remove the jumper wire between pins 1 and 2 and also pins 3 and 4 of power transformer T1. Install a jumper wire between pins 2 and 3 of the transformer and change Fuse F1 to a 0.125 amp slow blow.

CAUTION

Disconnect all power from the unit before changing voltages. Mark the unit to indicate it has been converted for 230 volt operation.

The Model 8230 is equipped with a standard three conductor power cord that automatically grounds the instrument when a matching power receptacle is available. An adapter which provides an instrument ground should be used whenever the power cord must be connected to a two-contact outlet.

2.4 Installation

The unit is normally supplied for bench top and tilt stand operation. If panel mounting is desired refer to paragraphs 2.6 and 2.7.

2.5 Initial Turn On

Initial Turn On should be accomplished as soon as possible after receipt of the instrument as part of the initial electrical inspection. This procedure checks the Model 8230 for any major internal shipping damage.

(1) Connect the instrument to an appropriate ac power source.

(2) Set the power switch to the On position--display illuminates.

(3) Continue through the steps of operation described in Chapter 3.

2.6 Tilt-Stand Removal

Figure 2-1 illustrates the procedure used to remove the tilt-stand. It is only necessary to remove the two tilt-stand retaining screws.

FIGURE 2-1

TILT-STAND REMOVAL AND INSTALLATION

2.7 Panel Installation/Cover Removal Procedure

This procedure is illustrated by Figure 2-2.

FIGURE 2-2

PANEL INSTALLATION/COVER REMOVAL PROCEDURE

This figure illustrates the procedure used (a) to remove the case and (b) to convert the Model 8230 to a panel mounted instrument. To convert the unit, it is only necessary to remove the two screws that hold the chassis, slip the chassis through the panel opening (3.110 in. high x 6.820 in. wide), and re-install the case to the chassis with the two rear panel mounted, case retaining screws.

CHAPTER 3

OPERATION

3.1 General

Since the Model 8230 is a fully automatic instrument, no preliminary adjustments are required and no operator controls are provided.

The only step necessary to bring the unit to a fully operational condition is to check that the front panel power switch is OFF, install the signal cable and power cord, and turn the power switch to ON (up position).

3.2 Operating Conditions

Operating temperatures should be limited as follows:

Maximum Temperature: 122°F (50°C)

Minimum Temperature: 32°F (0°C)

NOTE

Fuse F1 is indicated as 0.25 amp slow blow and labeled for 115 V ac operation. For 230 volt operation F1 is replaced with a 0.125 amp slow blow fuse and appropriately labeled.

CHAPTER 4

MAINTENANCE

4.1 Factory Service

Whenever the instrument requires service the nearest Systron-Donner representative should be contacted. He can provide field service or arrange for factory returns when necessary. Address all inquires on operation or applications to your nearest sales representative, or to:

Sales Manager
Data Products Division
Systron-Donner Corporation
888 Galindo Street
Concord, California 94520

Specify both model and complete serial number in all correspondence.

4.2 Routine Maintenance

A regular program for routine maintenance and inspection every five to six months is recommended for this unit. As part of these regular procedures, the instrument should be checked in the following manner:

(1) Disconnect ac power and remove instrument cover.

(2) Make a thorough visual inspection of all wiring and cables. Check for frayed, loose, or burned wires.

(3) Check for physical integrity of all components. Look for burned or cracked components, loose solder connections, leakage of insulation compounds, and general physical damage. Check that all integrated circuit packages are firmly

mounted. Never unnecessarily remove and replace a package.

(4) Check front panel switch for loose or broken terminals.

(5) If the internal panel surfaces and components have an excessive amount of dust deposited on them, use a soft brush and a low pressure stream of air to remove the foreign material.

CAUTION

Do not clean PC boards or small internal components with a stiff brush or solvents, since damage to the circuits may result. A high-powered vacuum cleaner device should not be used on small internal components.

(6) Wipe the external surfaces of the instrument with a soft damp cloth to remove dirt, fingerprints and other foreign material.

(7) Replace the cover and reconnect the ac power. Check operation. If performance does not match or exceed the specifications listed in Chapter I of this manual, corrective maintenance is in order.

4.3 Printed-Circuit Board Repair

To remove a part on the printed circuit board, cut the leads of the part near the lead holes. Using a low power (50 watts or less) soldering iron, apply heat sparingly to each cut lead.

As soon as the solder melts, slip the lead from the hole and clean the hole with a toothpick. Clean the board surfaces with isopropyl alcohol. Form the tinned leads of the replacement part and insert in cleaned holes, trimming the leads to extend 1/16 inch beyond the back surface of the board. Only 63/37 solder with a maximum diameter of 1/16 inch should be used. Solder the leads to the board and use a hemostat, iong-nosed pliers, or other heat sink on the leads of all semiconductor devices and quarter-watt resistors. Allow the soldered junction to cool before removing the heat sink.

WARNING

Dangerous high voltages are present in the power supply and display circuits of this unit. Use caution at all times when the protective cover is removed.

CHAPTER 5

FUNCTIONAL DESCRIPTION

5.1 General

The Model 8230 Time Code Reader Schematic Dwg. #31119-7-1 covers the complete instrument. It consists of four basic subsections: 1) the Code Stripper and Signal Conditioner section, 2) the Reader Logic section, 3) the Storage and Display section and, 4) the Power Supply. These will be described in that order.

When citing a sub-element of a multi-element integrated circuit in the following discussion, the reference designation of the IC chip is given, followed by the output pin number of the particular element in question. For example: A21-8 identifies the gate with output pin 8 on quad gate A21. When a flip-flop formed from two gates is cited, both output pins are used. For example: flip-flop A21-6, 3 identifies the flip-flop formed from gates A21-6 and A21-3. The first pin number given (pin 6) is the Q output.

5.2 Code Stripper and Signal Conditioner

The Code Stripper and Signal Conditioner section is shown at the upper left on Schematic 31119-7-1. This section accepts the amplitude modulated input signal, buffers it and separates it into two standardized (conditioned) trains of output signals; one representing the carrier and labeled EC (each cycle) and the

other representing the modulated code and labeled LC (large cycle). These signals are inverted and fed to the Reader Logic section.

The input signal is fed through BNC connector J2 and capacitor coupled through C1 to source follower Q1. This circuit serves as a buffer presenting a high impedance to the signal source and providing a low impedance output which is coupled through C2 and C5 to the LC and EC circuits, respectively.

The Code Stripper (consisting of Diodes CR13 and CR14, capacitor C3 and resistors R9 and R10) "strips" the coded information from the input signal. This information is contained in the large cycles. See line 1 of Timing Diagram Dwg. #31529-7-1. Capacitor C3 charges to the negative peaks (lower large half cycle peaks) of the input signal. Approximately 90% of this peak voltage across C3 appears at the junction of R9 and R10 setting the bias on CR13. Only the peak 10% of the lower large half cycles are permitted to pass through CR13 to the Signal Conditioning Circuit. The small cycles are well within the 90% bias level and are ignored.

The LC Signal Conditioner consists of Amplifier A25, Squaring Circuit Q2Q3 and inverter Q4. The amplifier has a closed loop gain of 50. Diode limiters around the amplifier keep the output within rated levels over the rated (0.75 volts to 20 volts

peak-to-peak) range of the input code. They permit the amplifier to saturate without overloading. The output of the amplifier is fed to the Squaring Circuit where it is sharpened and converted to a positive level signal. This signal is inverted by Q4 and fed to the Reader Logic as signal $\overline{LC}$. See line 3 of the Timing Diagram.

The EC Signal Conditioner is identical to the LC Conditioner circuit. It consists of Amplifier A26, Squaring Circuit Q5Q6 and Inverter Q7. The output ($\overline{EC}$ from Q7) is a square-wave which is synchronized with the input signal carrier. It is shown on line 2 of the Timing Diagram in proper phase relationship to the $\overline{LC}$ signal on line 3. Note that the $\overline{LC}$ pulses are narrower and fall between the leading and trailing edges of the $\overline{EC}$ pulses. This relationship is essential to proper operation of the Reader Logic. This will become clear as we proceed.

As mentioned above, only the lower large half cycles are passed through the Stripper. These were chosen because they are less subject to dropout and attenuation than the upper half cycles. Since the basic Model 8230 is a ripple through reader which is not updated "on time", it will also read an inverted code. In this case the upper half cycles (being inverted) are passed through the Stripper.

5.3 Reader Logic

The Reader Logic accepts the $\overline{EC}$ and $\overline{LC}$ signals from the Code Stripper and Signal Conditioner section; sorts out double MARKS, single MARKS, ONES and ZEROS; establishes synchronism with the time code frames; accumulates time data in two-digit increments of seconds, minutes and hours and generates strobe signals for the transfer of these data to the Storage and Display section at the proper times during each frame.

Reference to the IRIG A, B and E Time Code Formats in Chapter 6 and the representation of the modulated signal on line 1 of the Timing Diagram will disclose some fundamental characteristics which are essential to an understanding of the Reader Logic. Note that a MARK is defined by eight large cycles, a ONE by five large cycles and a ZERO by two large cycles. The leading edges of these groups of large cycles are spaced at precisely ten-cycle intervals with the gaps between the groups filled with small cycles. In the following discussion, these ten-cycle intervals are called "X-times". Each frame contains 100 X-time periods with MARKS separating them into ten equal periods called Y-times. The X-and Y-times are labeled 0 through 9 with X0 Y0 occuring at the beginning of the frame. The 1000 individual carrier cycles in each frame are called Z-times and are labeled 0 through 9 within each X-time period. A MARK is placed at the beginning of the frame

(X0 Y0 time) with its leading edge "on time". The remaining ten MARKS which define the Y-times are located in the X9 time slots in each of the ten Y-time periods. This results in a double MARK (two consecutive MARKS) at the beginning of each frame.

The Reader Logic counts the $\overline{LC}$ pulses. It interprets 7,8 or 9 pulses as a MARK; 4,5 or 6 pulses as a ONE and 1,2 or 3 pulses as a ZERO, thus achieving a measure of digital filtering. The MARKS are counted separately to establish Y-times. This Y-counter is reset whenever a double MARK is detected, synchronizing the reader with the time code frame. The Y-counter need only count to 3 and then "lock up" until cleared at the beginning of the next frame, since only the seconds, minutes and hours data, which are in the first three Y-time periods, are read from the code. The ONES and ZEROS are loaded into a serial-in/parallel-out shift register. This shift register is cleared and a ONE loaded in by the MARK at the beginning of the frame and subsequently, by the MARKS at the end of each Y-time period. This ONE is shifted through the shift register as the ONES and ZEROS in each X-time following the MARK are loaded in behind it. When it is detected in the last bit position of the shift register, one additional shift is permitted to occur dumping it off the end and a strobe pulse is generated which transfers the data in the shift register into one of three storage registers selected by the Y-counter.

These storage registers, one each for seconds, minutes and hours data, are part of the Storage and Display section.

Referring to the schematic and timing diagram, the above operation is achieved as follows: first a gating signal "A" (line 7) is developed which gates an EC half-cycle pulse "B" at the end of each group of $\overline{LC}$ pulses. Signal "A" is generated by flip-flop A20-3, 6. This flip-flop is set on the negative going transition of the $\overline{EC}$ signal. It is immediately reset if a $\overline{LC}$ pulse is present during that $\overline{EC}$ period. (This operation depends on the previously mentioned fact that the $\overline{LC}$ pulses are narrower and centered within the $\overline{EC}$ pulse times). At the end of each $\overline{LC}$ pulse group the flip-flop is <u>not</u> reset and "A" output stays up opening gate A23-8 to the next positive $\overline{EC}$ pulse. (The third input, "D", to A23-8 is up at this time). The inverse of this gated EC pulse appears as signal "B" at the output (line 8). Signal "B" sets flip-flop A20-11, 8 and holds "D" positive through A24-11 and A16-2. Signal "D" is shown on line 10. The output ("C" on line 9) of flip-flop A20-11, 8 is fed to the clock input (pin 8) to shift register A18.

During the above events, the $\overline{LC}$ pulses are fed through gate A24-3 and counted by decade A19. The 1-2-4 BCD outputs from A19 are fed to NAND gate A23-6. All three of these lines are up at a count of 7, driving A23-6 output ("F" on line 12) to ground and closing gate A24-3 to subsequent $\overline{LC}$ pulses.

Decade A19 is "locked up" and will remain in this condition until reset. This locked state is interpreted as a MARK and is established by a group of 7, 8 or 9 $\overline{LC}$ pulses. A ONE condition is established by the "4 bit" line (A19-8) going positive. This condition exists at counts of 4, 5 or 6. (It is also true at a count of 7, establishing the first ONE fed to the shift register when a MARK is decoded). The ONE (4 bit) line is fed to the input, pins 1 and 2, of shift register A18. A ZERO is interpreted as the absense of a ONE or a MARK. However, at least one $\overline{LC}$ pulse must be present. Thus, 1, 2 or 3 $\overline{LC}$ pulses represent a ZERO.

Decade A19 is reset when signal "D" goes to ground on the positive transition of "B". Signal "D" is ac coupled through C17 to inverter A16-4 resulting in signal "E" (line 11) at pins 2 and 3 of A19. Flip-flops A20-3, 6 and A20-11, 8 are reset by the first pulse in the next $\overline{LC}$ pulse group.

Next a reset signal "K" (line 16) is developed which goes to ground resetting the Y-counter (Dual Binary A15) whenever a double MARK is detected. This occurs at the beginning of each frame. Signal "K" emanates from three input NAND gate A22-8. All three inputs must be positive for "K" to go to ground. Each time a MARK is detected, signal "F" from A23-6 goes to ground, is inverted by A16-12 producing a positive input

"$\overline{F}$" to A22-8. In addition, signal "F" sets flip-flop A21-6, 3 driving output "G" (line 13) positive. Signal "G" opens gate A21-8 to the "$\overline{D}$" signal from A24-11. When "$\overline{D}$" goes positive, the output ("H" on line 14) from A21-8 goes to ground setting flip-flop A22-6, A21-11. The output from A22-6 ("J" on line 15) along with signal "D" from A16-2 are the two remaining inputs to A22-8. Output "K" does not go to ground at this time, however, because both the "D" and "$\overline{F}$" inputs have returned to ground. Flip-flop A21-6, 3 is reset by the first pulse in the next $\overline{LC}$ pulse group. If this $\overline{LC}$ group is a ONE or ZERO, flip-flop A22-6, A21-11 is reset by signal "B" from A23-8 and no "K" signal is produced. If it is a MARK, however, "K" goes to ground when the "$\overline{F}$" input goes positive ("D" is also positive at this time). Signal "K" is fed back to an input to A22-6 preventing this flip-flop from being reset by the next "B" pulse. It is reset by the one following it instead, since the next $\overline{LC}$ group will not be a MARK. The "K" signal returns positive when "$\overline{F}$" and "D" go to ground.

Signal "K" clamps the Y-counter in reset through pins 1 and 13 of A15. The input to the Y-counter is signal "L" (line 17) to the clock input to binary A15-5. It is derived from the three input AND gate formed from gate A22-12 and inverter A16-6. The $\overline{Y3}$ input from A13-3 goes positive when the Y-counter is reset (both the 1Y and 2Y outputs are at ground). The other two inputs,

"$\overline{F}$" to A22-8. In addition, signal "F" sets flip-flop A21-6, 3 driving output "G" (line 13) positive. Signal "G" opens gate A21-8 to the "$\overline{D}$" signal from A24-11. When "$\overline{D}$" goes positive, the output ("H" on line 14) from A21-8 goes to ground setting flip-flop A22-6, A21-11. The output from A22-6 ("J" on line 15) along with signal "D" from A16-2 are the two remaining inputs to A22-8. Output "K" does not go to ground at this time, however, because both the "D" and "$\overline{F}$" inputs have returned to ground. Flip-flop A21-6, 3 is reset by the first pulse in the next $\overline{LC}$ pulse group. If this $\overline{LC}$ group is a ONE or ZERO, flip-flop A22-6, A21-11 is reset by signal "B" from A23-8 and no "K" signal is produced. If it is a MARK, however, "K" goes to ground when the "$\overline{F}$" input goes positive ("D" is also positive at this time). Signal "K" is fed back to an input to A22-6 preventing this flip-flop from being reset by the next "B" pulse. It is reset by the one following it instead, since the next $\overline{LC}$ group will not be a MARK. The "K" signal returns positive when "$\overline{F}$" and "D" go to ground.

Signal "K" clamps the Y-counter in reset through pins 1 and 13 of A15. The input to the Y-counter is signal "L" (line 17) to the clock input to binary A15-5. It is derived from the three input AND gate formed from gate A22-12 and inverter A16-6. The $\overline{Y3}$ input from A13-3 goes positive when the Y-counter is reset (both the 1Y and 2Y outputs are at ground). The other two inputs,

"$\overline{F}$" and "C", are both positive during the "B" signal time whenever a MARK is detected. A total of four "L" pulses are generated during each frame. The first of these, associated with the "X0Y0 MARK", is ignored since the Y-counter is being held reset by "K" when it occurs. Thus, the Y-counter is in the binary 00 state until advanced to the 01 state by the "L" pulse associated with the X9Y0 MARK. In like manner, it is advanced through the binary 10 to the 11 state by the "L" pulses associated with the X9Y1 and X9Y2 MARKS, respectively. When the X9Y2 MARK occurs both the 1Y and 2Y inputs to gate A13-3 are positive and the output, $\overline{Y3}$, goes to ground closing gate A22-12. No more "L" pulses are generated and the Y-counter stays in the 11 state until reset by the next "K" pulse.

The Y-counter outputs (1Y and 2Y) are decoded by NAND gates A14-12-6 and -8 into Y0, Y1 and Y2 signals, respectively, which are gated during the Data Strobe time. These gated signals, labeled $\overline{SbY0}$, $\overline{SbY1}$ and $\overline{SbY2}$ are inverted and buffered by drivers A13-10, -4 and -11, respectively. The resulting signals are fed to the storage registers in the Storage and Display section for the updating of seconds, minutes and hours data.

The "$\overline{F}$" signal is also fed to a two input NAND gate, formed from AND gate 24-6 and inverter A16-10, opening it to "$\overline{A}$" signals from A20-6. The resulting output "M" (line 18) goes to ground whenever a MARK is detected. It is fed to the

clear input (pin 9) to shift register A18 returning all outputs to zero during the early part of each "F" signal time. The "M" signal returns positive prior to the occurance of the shift signal "C" associated with the MARK and a ONE is loaded into the shift register at this time. This ONE appears at Q1 output (pin 3) of A18. It is shifted to output Q2 and so on as each subsequent bit is decoded and loaded into the shift register. When it reaches Q8, on shift 8 of signal "C", this output (labeled "P" and shown on line 24 of the timing diagram) goes positive. Signal "P" is fed to three input NAND gate A23-12. The other two inputs to this gate are "$\overline{C}$" and "T" (line 28). Signal "T" emanates from flip-flop A17-11, 8. It is positive at this time since the flip-flop was set by clear signal "M" (line 22). When "$\overline{C}$" goes positive (at X8Y0, X7Y1 or X7Y2 time) the output of A23-12 goes to ground setting flip-flop A17-6, 3. The output "R" (line 26) goes positive opening AND gate A24-8 to the ninth shift pulse ("C" on line 19). When this occurs, output "S" goes positive, is inverted by A16-8 resetting flip-flop A17-11,8 and returning signal "T" to ground. Flip-flop A17-6, 3 is reset when "D" goes to ground one-half Z-time later (see lines 9 and 10) returning "R" and "S" to ground. The ninth shift pulse, which caused the above events, loads the last data bit of interest into the shift register dumping the ONE which was in the Q8 position off the end. The "S" pulse is

used as the Data Strobe mentioned previously. It directs the loading of the contents of the shift register into the appropriate storage register.

5.4 Storage and Display

The Storage and Display section is shown at the upper right on Schematic 31119-7-1. This section accepts the parallel BCD data at the outputs of the shift register (A18) in two digit increments of seconds, minutes and hours, stores these data on command from the Reader Logic section and converts the stored BCD data to ten line for display on Numerical Indicator tubes. The seconds, minutes and hours segments of the six digit display are separated by lighted colons to reduce the possibility of misinterpretation.

The BCD data is stored in a register consisting of six quad latch elements, A7 through A12. Each quad latch can store up to four bits. Bits present at input pins 2, 3, 6 and 7 are transferred to output pins 16, 15, 10 and 9, respectively, when the strobe input, to pins 13 and 4, goes positive. When this strobe line returns to ground, the bits on the outputs at that time are stored. These outputs are no longer affected by changes at the inputs as long as the strobe line remains at ground. The seconds, minutes and hours strobe pulses from buffers A13-10, -4 and -11, respectively, are generated in sequence updating each section of the storage register as the associated data is accumulated during each frame.

The parallel BCD outputs from the storage register are fed to Numerical Indicator Tube drivers A1 through A6 where they are converted to ten line form to drive Numerical Indicator tubes V1 through V6, respectively. The display is in group decimal 23:59:59 full scale.

5.5 Power Supply

The Power Supply is shown in the lower left on Schematic 31119-7-1. It provides regulated +5 volts (Vcc), unregulated ±10 volts for the Signal Conditioner amplifier and unregulated +225 volts for the Numerical Indicator tubes and neon lamps. An adjustment, R40, is provided for the regulated +5 volts. The power transformer has split primary windings which are connected in parallel for 115 volt operation and in series for 230 volt operation. The input line is three-wire, with the third wire grounded to the chassis. Both sides of the line are filtered and the hot wire is fused. This fuse, F1, is 0.25 A Slow Blow for 115 volt operation and 0.125 A Slow Blow for 230 volt operation.

CHAPTER 6

PARTS LIST AND ILLUSTRATIONS

6.1 Parts List

Final Assembly Time Code Reader

Ref.	Description	S-D Part No.
F1	Fuse, 1/4 Amp.	F0043
J1	Line Filter Assembly	21981-4-1
J2	Connector BNC	J0165
XF1	Fuse Holder	X0034
	Transistor, 2N4921	Q0267

Line Filter Assembly (Dwg. #21981-4-1)

C1,2	Capacitor, 0.01 µf, 500 V	C0423
J1	Reset AC Switchcraft AC36	J0566
L1,2	Hash Filter (JW Miller #5250)	L0166
	Terminal	E0141

Front Panel Assembly

	Capacitor, 10 µf, 450 V	C0337
	Capacitor, 2500 µf	C1148
	Transformer	25294
	Standoff	E0098
DS1-4	Lamp Neon (Los Angeles Min Prod #95)	10086
S1	Switch Toggle (CK7101)	S0149
	Terminal Feedthru (CTC 4182-2-0119)	E0316

Assembly Time Code Reader (Dwg. #31119-4-1)

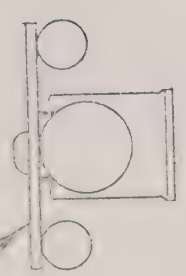
A1-6	IC, SN7441N	19707
A7-12	IC, SN7075N	25731
A13	IC, MC857P	
A14,22,23	IC, SN15862N	19719
A15	IC, SN7474N	25241

Assembly Time Code Reader (cont)

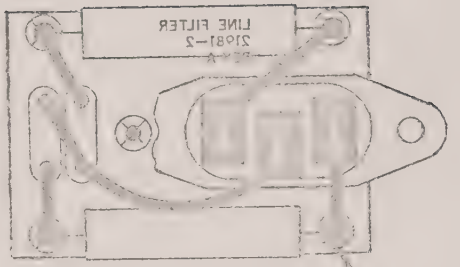
Ref.	Description	S-D Part No.
A16	IC, MC836P	25704
A17,20,21	IC, SN15846N	19716
A18	IC, DM8570N	
A19	IC, SN7090N	25732
A24	IC, MC1806P	25733
A25,26	IC, LM201H	
C1	Capacitor, 0.01 µf, DISC	C0423
C2,3	Capacitor, 0.47 µf, 35 V	C0982
C4,7,9	Capacitor, 4.7 µf, 10 V	C1011
C5	Capacitor, 4.7 µf, 35 V	C0406
C6,8	Capacitor, 5 pf, dipped, El Menco	DM10-050J
C10	Capacitor, 100 µf, 20 V	C1025
C11	Capacitor, 125 µf, 10 V	C1147
C12	Capacitor, 39 µf, 20 V, SPR 150D	150D396X9020R2
C15,16	Capacitor, 1000 pf	C0543
CR1	Diode, IN971B	CR0229
CR2-7,10,11	Diode, IN4005	CR0284
CR8	Diode, 19330	19330
CR9	Diode, IN749A	CR0306
CR12-19	Diode, IN4151	CR0150
L1,2	Inductor, R45-4	L0143
R1,3,4,10	Resistor, 100 kΩ, 1/4 W, 5%, CC	R0741
R2	Resistor, 1 MΩ, 1/4 W, 5%, CC	R0962
R5	Resistor, 68 kΩ, 1/2 W, 5%, CC	R0273
R6	Resistor, 8.2 kΩ, 1/4 W, 5%, CC	R0883
R7	Resistor, 2 kΩ, 1/4 W, 5%, CC	R0734
R8	Resistor, 110 kΩ, 1/4 W, 5%, CC	R1010
R9,11,25,31	Resistor, 10 kΩ, 1/4 W, 5%, CC	R0766
R12,26	Resistor, 510 kΩ, 1/4 W, 5%, CC	R0968
R13,16,20,27, 30,35	Resistor, 1 kΩ, 1/4 W, 5%, CC	R0765
R14,15,28,29	Resistor, 5.1 kΩ, 1/4 W, 5%, CC	R0693
R17,18,22,32, 36	Resistor, 4.7 kΩ, 1/4 W, 5%, CC	R0892

Assembly Line Code Boards (cont.)

Ref.	Description	S-D Part No.
R19	Resistor, 3.3 kΩ, 1/4 W, 5%	R0742
R21,23,24,33, 34,37,38	Resistor, 5.6 kΩ, 1/4 W, 5%, CC	R0821
R39	Resistor, 330 Ω, 1/4 W, 5%, CC	R0662
R40	Potentiometer, 100 Ω	R2374
R41,42,43	Resistor, 3.9 kΩ, 1/4 W, 5%, CC	R0939
R44-49	Resistor, 39 kΩ, 1/2 W, 5%, CC	R0282
R50-53	Resistor, 330 kΩ, 1/4 W, 5%	R1203
Q1	Transistor, MPF152	Q0263
Q4	Transistor, 2N4124	Q0235
Q8	Transistor, 2N3643	Q0179
Q2,3,5,6	Transistor, 2N4126	Q0236
V1-6	Tube Readout (NL904)	V0125

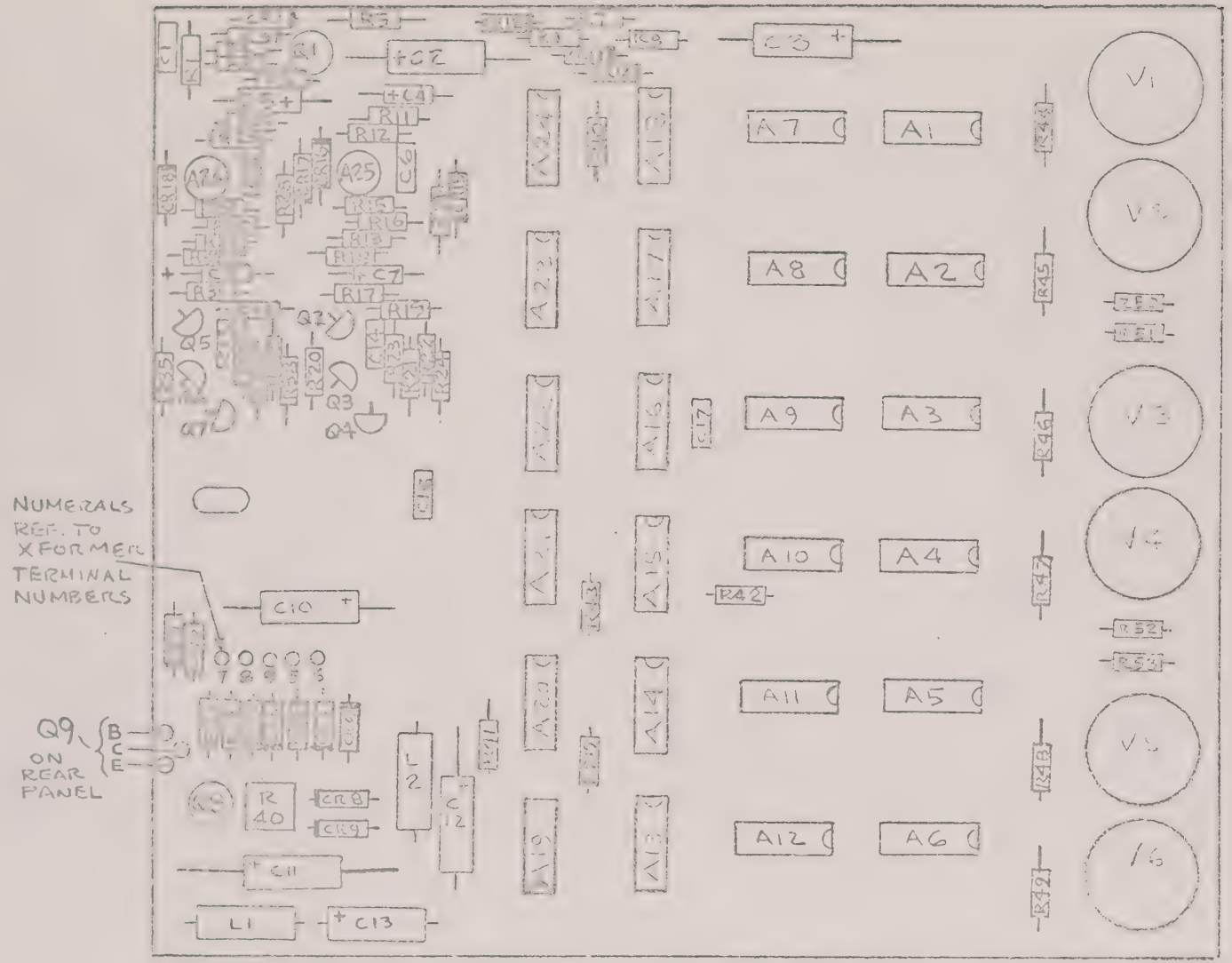


C.KT SIDE
OF BOARD

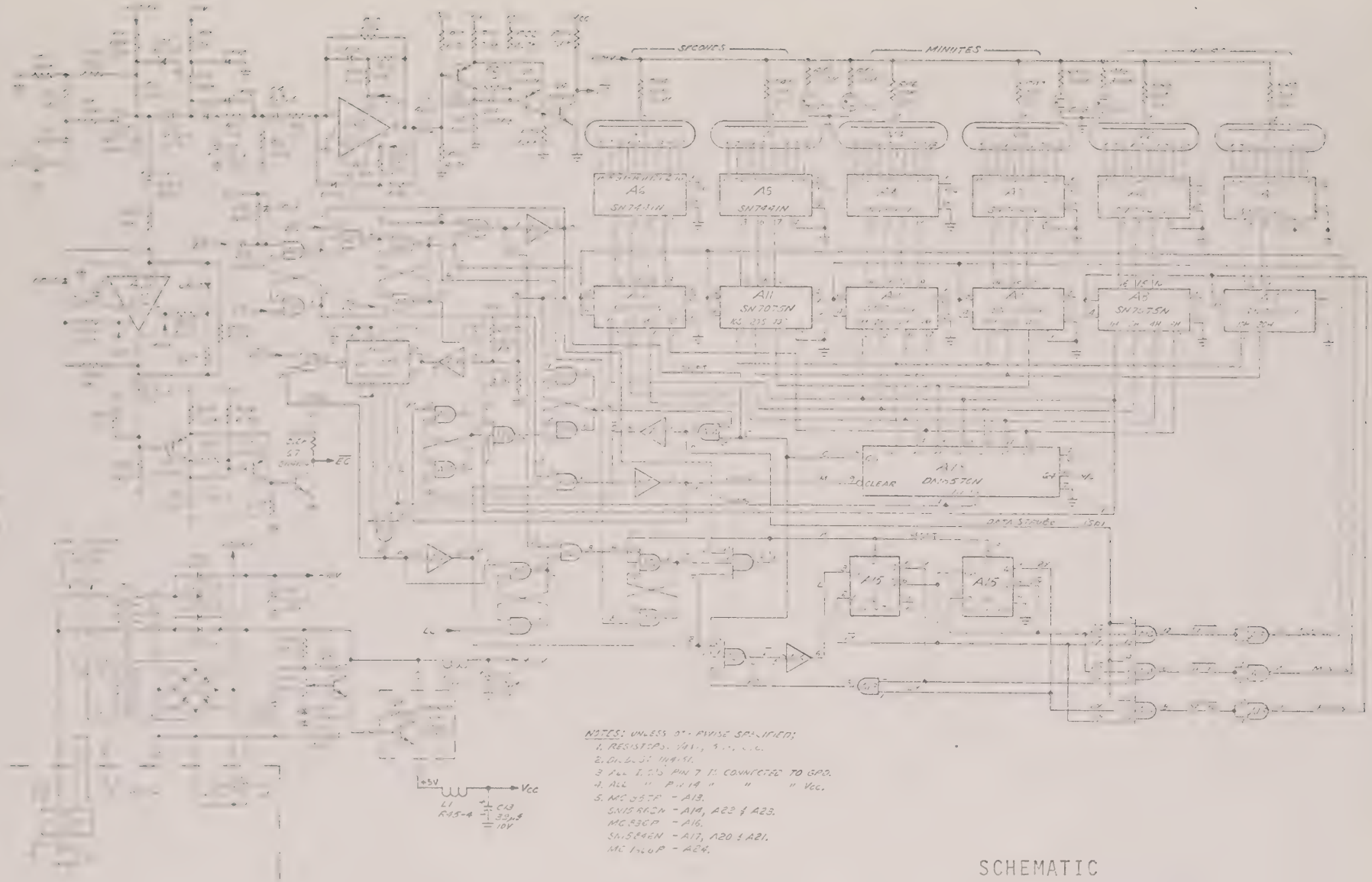


E-0141 TERMINAL
5 PLACES

ASSEMBLY
LINE FILTER
21981-4-1 A

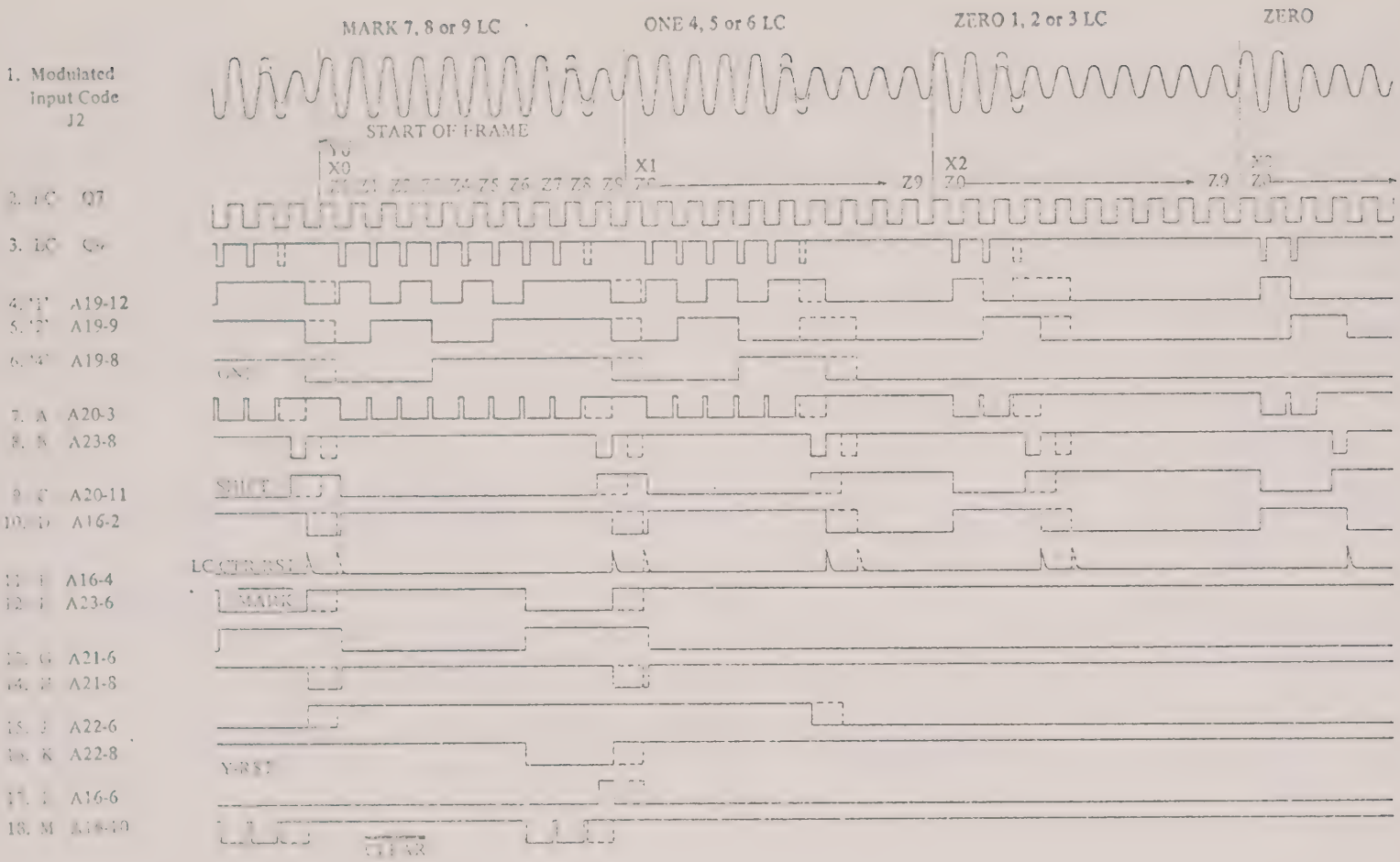


ASSEMBLY
MODEL 8230 IRIG B
TIME CODE READER
31119-4-1 B



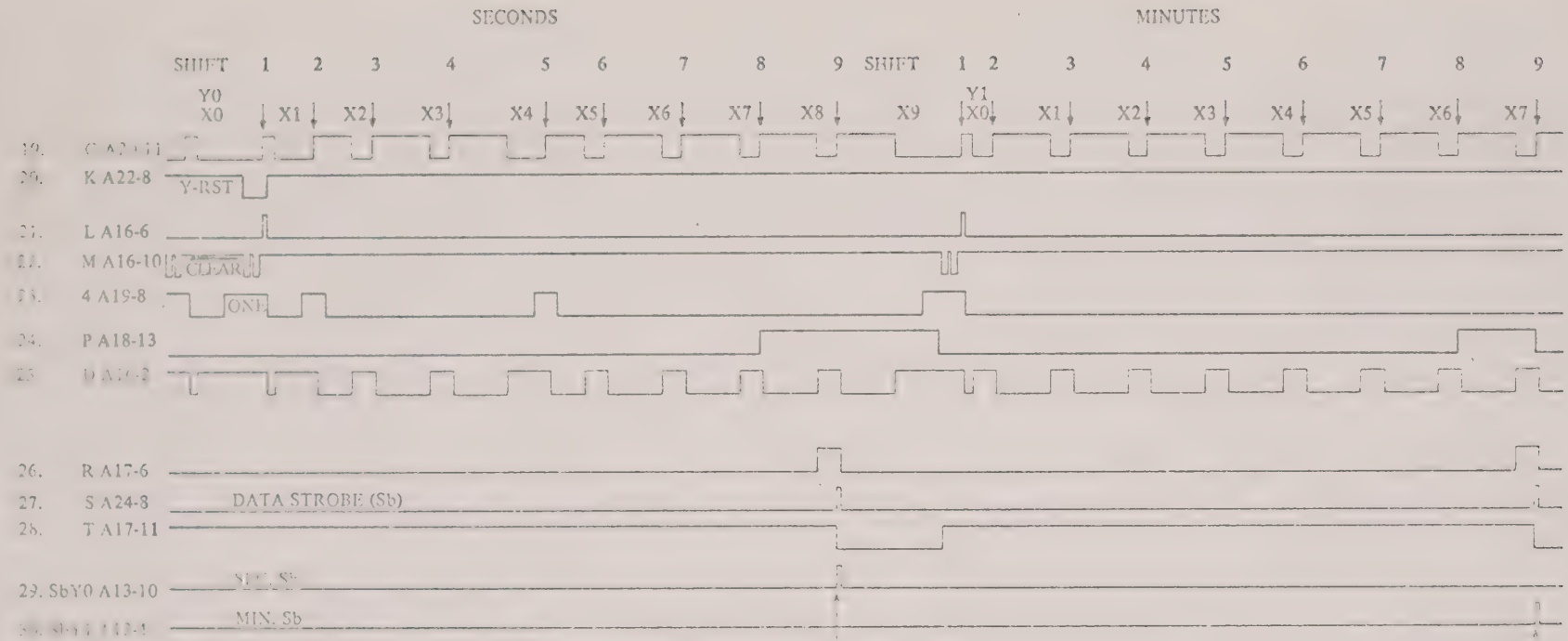
NOTES: UNLESS OTHERWISE SPECIFIED:
1. RESISTORS: 1/4W, 5%, CC.
2. DIODES: 1N4151.
3. ALL I.C.'S PIN 7 IS CONNECTED TO GND.
4. ALL " PIN 14 " " " Vcc.
5. MC355P - A13.
SN5493N - A14, A22 & A23.
MC830P - A16.
SN5496N - A17, A20 & A21.
MC1408P - A24.

SCHEMATIC
MODEL 8230 IRIG B
TIME CODE READER
31119-7-1 B



NOTE: DOTTED LINES INDICATE EFFECT OF ONE EXTRA LARGE CYCLE FOR EACH BIT.

MODEL 8230 IRIG B
TIMING DIAGRAM
31529-7-1 Sheet 1



Contents of Shift Register at Shift 9 time

09 SECONDS

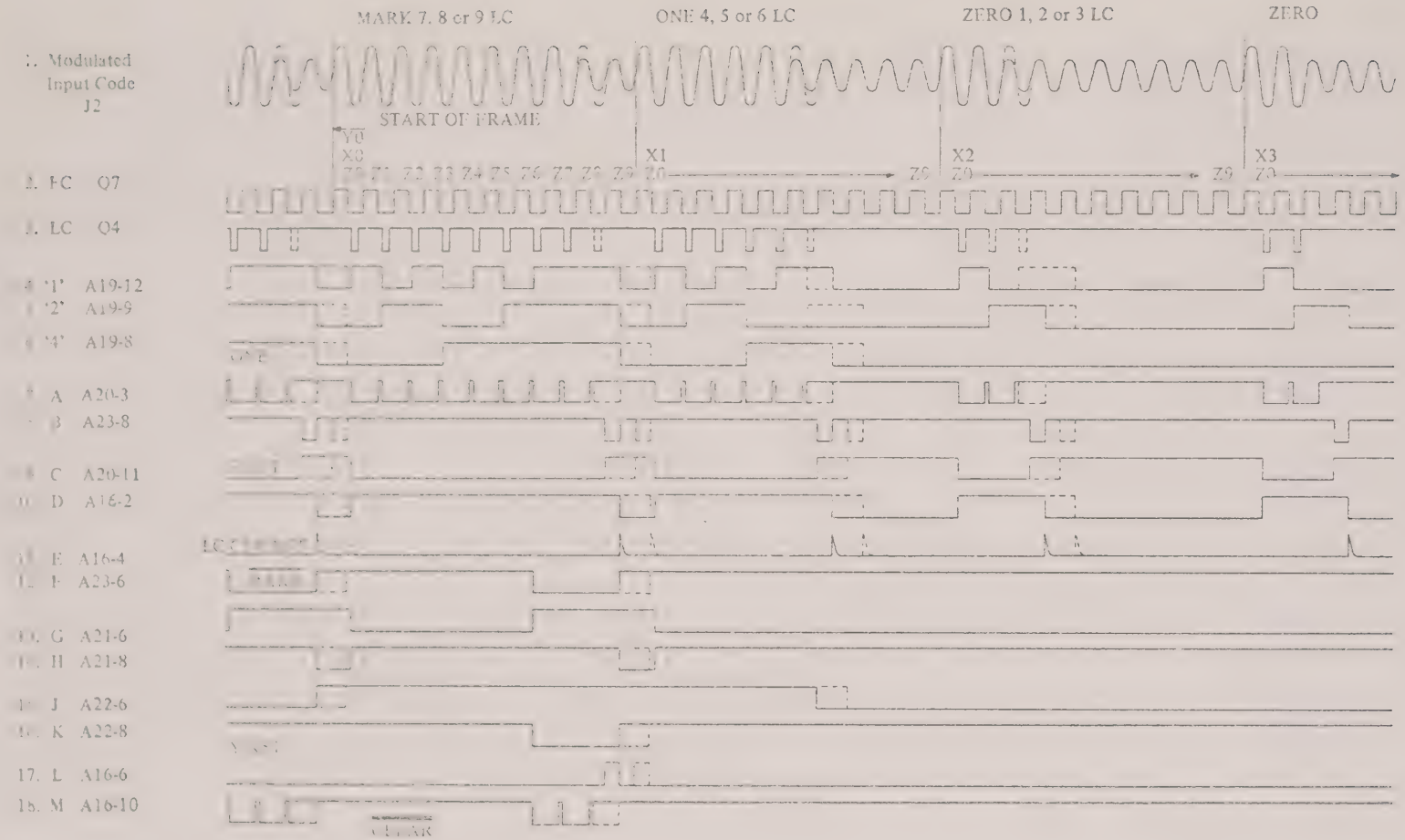
M	Q8	0
M	Q7	0
M	Q6	0
M	Q5	0
Dummy	Q4	0
M	Q3	0
M	Q2	0
M	Q1	0

Contents of Shift Register at Shift 9 time

00 MINUTES

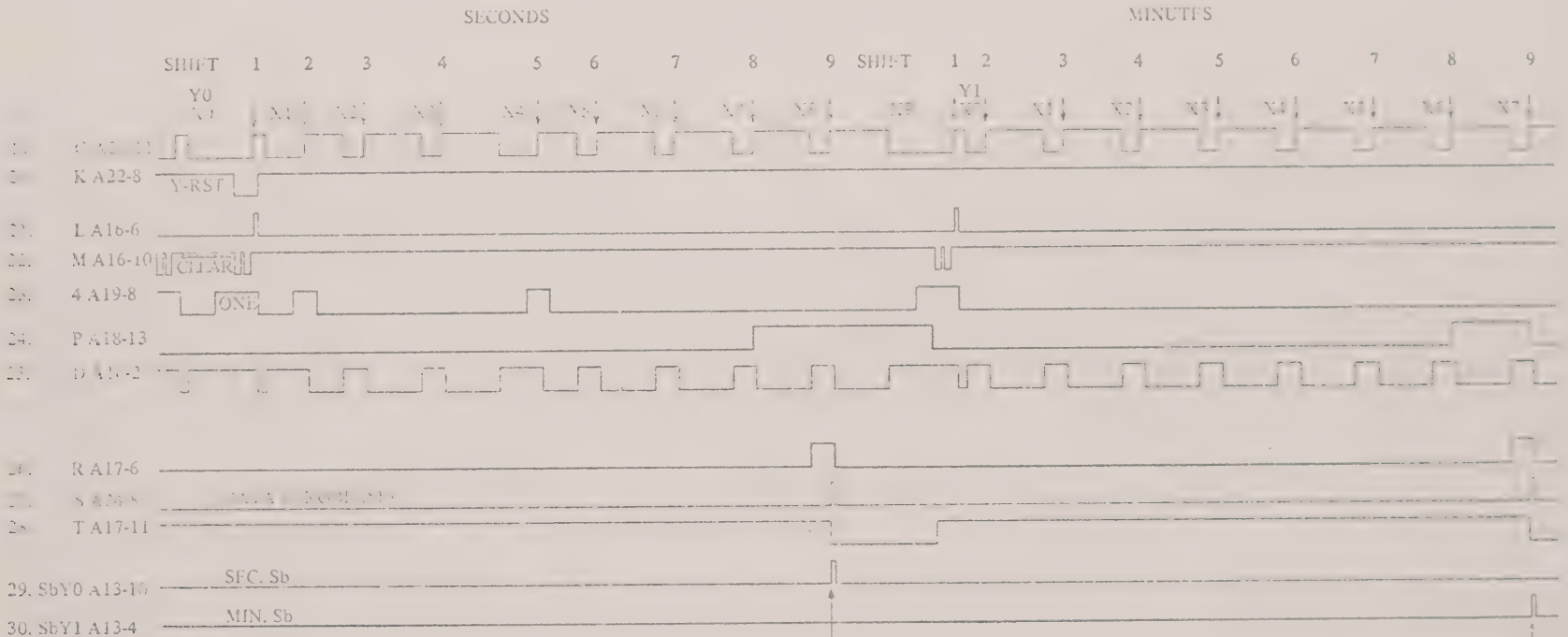
M	Q8	0
M	Q7	0
M	Q6	0
M	Q5	0
Dummy	Q4	0
M	Q3	0
M	Q2	0
M	Q1	0

MODEL 8230 IRIG B
TIMING DIAGRAM
31529-7-1 Sheet 2



NOTE: DOTTED LINES INDICATE EFFECT OF ONE EXTRA LARGE CYCLE FOR EACH BIT.

MODEL 8230 IRIG B
TIMING DIAGRAM
31529-7-1 Sheet 1



Contents of Shift Register at Shift 9 time

09 SECONDS

M	Q8	0
M	Q7	0
M	Q6	0
M	Q5	0
Dummy	Q4	0
M	Q3	0
M	Q2	0
M	Q1	0

Contents of Shift Register at Shift 9 time

00 MINUTES

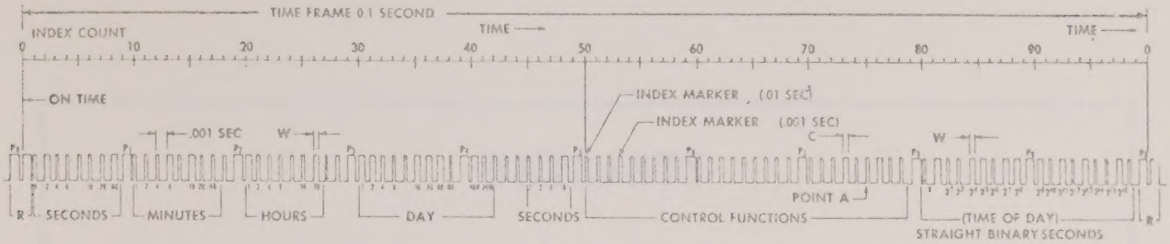
M	Q8	0
M	Q7	0
M	Q6	0
M	Q5	0
Dummy	Q4	0
M	Q3	0
M	Q2	0
M	Q1	0

MODEL 8230 IRIG B
TIMING DIAGRAM
31529-7-1 Sheet 2

IRIG TIME CODE FORMATS

FORMAT A

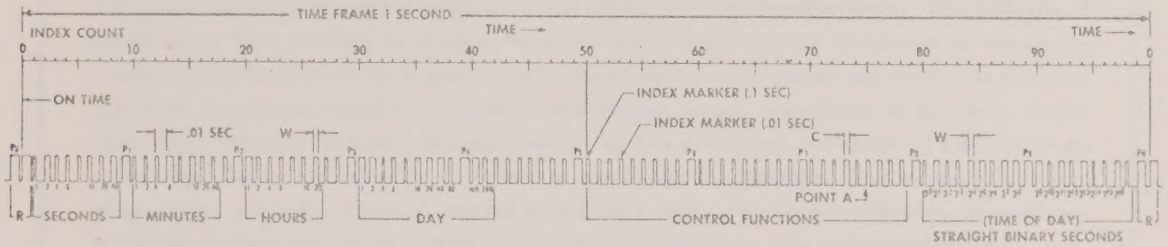
1000-PPS, 34-BIT BCD TIME-OF-YEAR/17-BIT BINARY TIME-OF-DAY CODE



TIME AT POINT A = 21:18:42 + .8 + .07 + .005 = 21 HR. 18 MIN. 42.875 SEC. ON DAY 173

FORMAT B

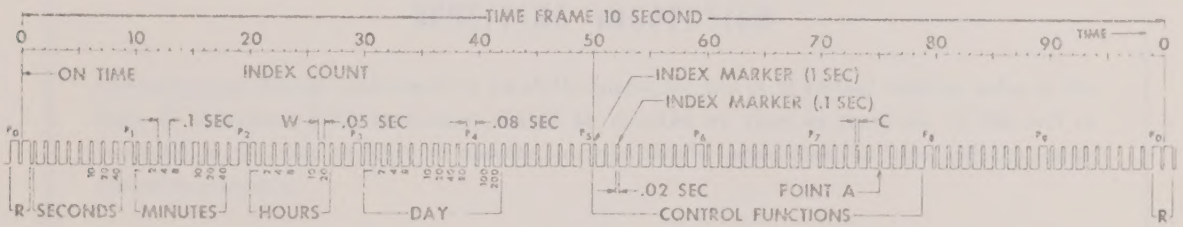
100-PPS, 30-BIT BCD TIME-OF-YEAR/17-BIT BINARY TIME-OF-DAY CODE



TIME AT POINT A = 21:18:42 + .7 + .05 = 21 HRS. 18 MIN. 42.75 SEC. ON DAY 173

FORMAT E

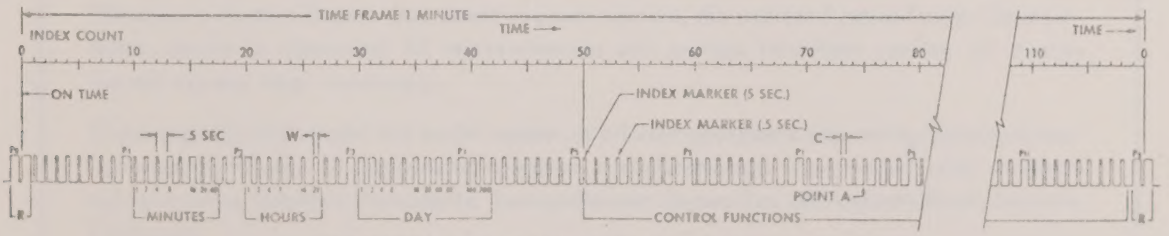
10-PPS, 26-BIT BCD TIME-OF-YEAR CODE



TIME AT POINT A = 21:18:40 + .7 + .5 = 21 HR. 18 MIN. 47.5 SEC. ON DAY 173

FORMAT C

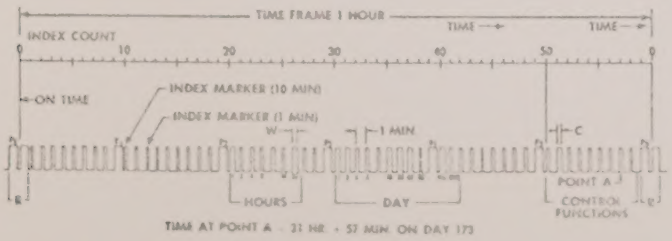
2-PPS, 23-BIT BCD TIME-OF-YEAR CODE



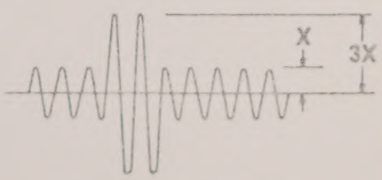
TIME AT POINT A = 21:18 + 37.5 SEC. = 21 HRS. 18 MIN. 37.5 SEC. ON DAY 173

FORMAT D

1-PPM, 16-BIT BCD TIME-OF-YEAR CODE



TIME AT POINT A = 21 HR. + 57 MIN. ON DAY 173



TYPICAL MODULATED SIGNAL

WARRANTY

Systron-Donner instruments are warranted during a period of one year from date of shipment to original purchaser to be free from defects in material and workmanship. This warranty does not apply to vacuum tubes, except as they are warranted by tube manufacturers. The liability of Seller under this warranty is limited to replacing or repairing any instrument or component thereof which is returned by Buyer at his expense during such period and which has not been subjected to misuse, neglect, improper installations, repair, alteration, or accident. Seller shall have the right of final determination as to the existence and cause of a defect. In no event shall Seller be liable for collateral or consequential damages. This warranty is in lieu of any other warranty, express, implied or statutory, and no agreement extending or modifying it will be binding upon Seller unless in writing and signed by a duly authorized officer.

RECEIVING INSPECTION

Every Systron Donner instrument is carefully inspected and is in perfect working order at the time of shipment. Each instrument should be checked as soon as received. If the unit is damaged in any way or fails to operate, a claim should immediately be filed with the transportation company.

REPAIRS

Whenever a Systron-Donner instrument requires service, the nearest Systron-Donner representative should be contacted; all representatives will provide immediate service or arrange factory returns when necessary.

Please specify both model and serial number in all correspondence concerning Systron-Donner instruments. Address all inquiries on operation or applications to your nearest sales representative or Sales Manager, Instruments, Systron-Donner Corporation, 888 Galindo Street, Concord, California.

MP MASTER
MA34106

MP-77369